CLAIMS

What is claimed is:

1. An electronic system, comprising:

critical circuitry;

non-critical circuitry having a first section and a second section; and

a power sub-system having a first power assembly, a second power assembly, and a set of connections which is configured to connect the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry.

2. The electronic system of claim 1 wherein the first section of the non-critical circuitry includes a first set of storage devices, wherein the second section of the non-critical circuitry includes a second set of storage devices, wherein the electronic system operates as a data storage system that stores data into and retrieves data from the first and second sets of storage devices on behalf of a host, and wherein the critical circuitry includes cache memory that temporarily buffers data exchanged between the host and the first and second sets of storage devices.

3. The electronic system of claim 2 wherein the second set of storage devices is configured to mirror data on the first set of storage devices.

4. The electronic system of claim 2 wherein the first section of the non-critical circuitry further includes:

a first front-end interface that is configured to operate as an interface between the host and the cache memory, and

a first back-end interface that is configured to operate as an interface between the cache memory and the first set of storage devices; and

wherein the second section of the non-critical circuitry further includes:

a second front-end interface that is configured to operate as an interface between the host and the cache memory, and

a second back-end interface that is configured to operate as an interface between the cache memory and the second set of storage devices.

5. The electronic system of claim 4 wherein the set of connections of the power sub-system includes:

a first interconnect that electrically connects to the first set of storage devices;

a second interconnect that electrically connects to the second set of storage devices;

a third interconnect that electrically connects to the cache memory, the first front-end and back-end interfaces, and the second front-end and back-end interfaces;

a first bus bar assembly that electrically connects the first power assembly to the first and third interconnects; and

a second bus bar assembly that electrically connects the second power assembly to the second and third interconnects.

6. The electronic system of claim 5 wherein the third interconnect includes:

a backplane having columns of connectors, each column of connectors electrically connecting to one of the first front-end interface, the first back-end interface, the second front-end interface, the second back-end interface and the cache memory;

wherein the first bus bar assembly includes:

a first bus bar that electrically connects the first power assembly to the columns of connectors that electrically connect to the first front-end interface, the first back-end interface and the cache memory without electrically connecting the first power assembly to the columns of connectors that electrically connect to the second front-end interface and the second back-end interface; and

wherein the second bus bar assembly includes:

a second bus bar that electrically connects the second power assembly to the columns of connectors that electrically connect to the second front-end interface, the second back-end interface and the cache memory without electrically connecting to the columns of connectors that electrically connect to the first front-end interface and the first back-end interface.

7. The electronic system of claim 1 wherein X and Y are integers greater than 0; wherein the first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail; and wherein the second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

8. The electronic system of claim 1, further comprising:

a switch which is interconnected between the first and second power assemblies to voltage balance outputs of the first and second power assemblies.

9. The electronic system of claim 1 wherein the first power assembly of the power sub-system includes:

a first set of main power line connectors to connect to a first main power feed, and

a first set of auxiliary power line connectors to connect to a first auxiliary power feed; and

wherein the second power assembly of the power sub-system includes:

a second set of main power line connectors to connect to a second main power feed, and

a second set of auxiliary power line connectors to connect to a second auxiliary power feed.

10. The electronic system of claim 1 wherein the first section of the non-critical circuitry further includes:

a first fan assembly that removes heat from the first section of the non-critical circuitry, and

a second fan assembly that removes heat from the second section of the non-critical circuitry; and

wherein the second section of the non-critical circuitry further includes:

a third fan assembly that removes heat from the first section of the non-critical circuitry, and

a fourth fan assembly that removes heat from the second section of the non-critical circuitry.

11. The electronic system of claim 1 wherein the first section of the non-critical circuitry further includes:

a first service processor that provides user access and control to the electronic system; and

wherein the second section of the non-critical circuitry further includes:

a second service processor that provides user access and control to the electronic system.

12. A power system for providing power to electronics including critical circuitry and non-critical circuitry, the power system comprising:

a first power assembly;

a second power assembly; and

a set of connections which is configured to connect the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry.

13. The power system of claim 12 wherein the first section of the non-critical circuitry includes a first set of storage devices, wherein the second section of the non-critical circuitry includes a second set of storage devices, wherein the critical circuitry includes cache memory to temporarily buffer data exchanged between a host and the first and second sets of storage devices, and wherein the set of connections includes:

a first interconnect that is configured to electrically connect to the first set of storage devices;

a second interconnect that is configured to electrically connect to the second set of storage devices;

a third interconnect that is configured to electrically connect to the cache memory;

a first bus bar assembly that electrically connects the first power assembly to the first and third interconnects; and

a second bus bar assembly that electrically connects the second power assembly to the second and third interconnects.

14. The power system of claim 13 wherein the first section of non-critical circuitry further includes a first front-end interface which operates as an interface between the host and the cache memory, and a first back-end interface which operates as an interface between the cache memory and the first set of storage devices; wherein the second section of non-critical circuitry further includes a second front-end interface which operates as an interface between the host and the cache memory, and a second back-end interface which operates as an interface between the cache memory and the second set of storage devices; wherein the third interconnect includes:

a backplane having columns of connectors, each column of connectors being configured to electrically connect to one of the first front-end interface, the first back-end interface, the second front-end interface, the second back-end interface and the cache memory;

wherein the first bus bar assembly includes:

a first bus bar that electrically connects the first power assembly to the columns of connectors that are configured to electrically connect to the first front-end interface, the first back-end interface and the cache memory without electrically connecting the first power assembly to the columns of connectors that are configured to electrically connect to the second front-end interface and the second back-end interface; and

wherein the second bus bar assembly includes:

a second bus bar that electrically connects the second power assembly to the columns of connectors that are configured to electrically connect to the second front-end interface, the second back-end interface and the cache memory without electrically connecting to the columns of connectors that are configured to

electrically connect to the first front-end interface and the first back-end interface.

15. The power system of claim 12 wherein X and Y are integers greater than 0; wherein the first power assembly includes multiple first power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than X first power supplies fail; and wherein the second power assembly includes multiple second power supplies that perform a normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail, and an error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry when more than Y second power supplies fail.

16. The power system of claim 12, further comprising:

a switch which is interconnected between the first and second power assemblies to voltage balance outputs of the first and second power assemblies.

17. The power system of claim 12 wherein the first power assembly includes:

a first set of main power line connectors to connect to a first main power feed, and

a first set of auxiliary power line connectors to connect to a first auxiliary power feed; and

wherein the second power assembly includes:

a second set of main power line connectors to connect to a second main power feed, and

a second set of auxiliary power line connectors to connect to a second auxiliary power feed.

18. A method for providing power to electronics including critical circuitry and non-critical circuitry, the method comprising the steps of:

operating a first power assembly to power the critical circuitry and a first section of the non-critical circuitry;

operating a second power assembly to power the critical circuitry and a second section of the non-critical circuitry;

in response to a failure of the second power assembly, continuing to power the critical circuitry and the first section of the non-critical circuitry using the first power assembly; and

in response to a failure of the first power assembly, continuing to power the critical circuitry and the second section of the non-critical circuitry using the second power assembly.

19. The method of claim 18 wherein X and Y are integers greater than 0; wherein the first power assembly includes multiple first power supplies; wherein the step of operating the first power assembly includes the step of:

performing a first normal operating procedure to provide power to the critical circuitry and to the first section of the non-critical circuitry when up to X first power supplies fail;

wherein the step of operating the second power assembly includes the step of:

performing a second normal operating procedure to provide power to the critical circuitry and to the second section of the non-critical circuitry when up to Y second power supplies fail;

wherein the step of continuing to power the critical circuitry and the first section of the non-critical circuitry using the first power assembly in response to a failure of the second power assembly includes the step of:

performing a first error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry using the first power assembly when more than X first power supplies fail; and

wherein the step of continuing to power the critical circuitry and the second section of the non-critical circuitry using the second power assembly in response to a failure of the first power assembly includes the step of:

performing a second error handling procedure to discontinue providing power to the critical circuitry and to the first section of the non-critical circuitry using the second power assembly when more than Y second power supplies fail.

20. The method of claim 18, further comprising the step of:

interconnecting the first and second power assemblies through a switch to voltage balance outputs of the first and second power assemblies.

21. The method of claim 18, further comprising the steps of:

connecting a first set of main power line connectors of the first power assembly to a first main power feed;

connecting a first set of auxiliary power line connectors of the first power assembly to a first auxiliary power feed;

connecting a second set of main power line connectors of the second power assembly to a second main power feed; and

connecting a second set of auxiliary power line connectors of the second power assembly to a second auxiliary power feed.

22. An electronic system, comprising:

critical circuitry;

non-critical circuitry having a first section and a second section; and

a power sub-system having:

(a) a first power assembly,

(b) a second power assembly, and

(c) means for connecting the first and second power assemblies to the critical circuitry and the non-critical circuitry such that, when the first and second power assemblies operate to power the critical and non-critical circuitry through the set of connections, (i) a failure of only the second power assembly results in the first power assembly continuing to power the critical circuitry and the first section of the non-critical circuitry, and (ii) a failure of only the first power assembly results in the second power assembly continuing to power the critical circuitry and the second section of the non-critical circuitry.